Letters

Comments on GaAs MESFET Baseband-to-Microwave Passive Switches

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In two recent publications on broad-band passive GaAs MESFET switches [1], [2], Schindler and colleagues presented the low-power, low-frequency characteristics of these useful components. While complete characteristics were presented over the microwave spectrum, power-handling capability was not presented below 3 GHz. This letter emphasizes that the power-handling capability, as well as related nonlinearities such as total harmonic distortion, degrades significantly at lower frequencies in previously reported GaAs MESFET switches, and we expect similar characteristics in these recently reported switches as well. While this power-handling reduction is not significant for most RF and microwave users, there are negative implications for broad-band, baseband applications such as instrumentation and signal processing.

Data presented by commercial suppliers of such switches (for example M/A-COM, Tachonics, and Anzac) typically indicate a 10 dB decrease in 1 dB signal compression at a frequency near 50 MHz. The power handling is relatively frequency independent above 100 MHz and below 20 MHz. This decrease in power handling at low frequency is attributed to the gate bias circuit. A large resistor (usually 2 to 10 kΩ) is placed in the gate circuit to allow the gate to float at the average channel potential. At low frequencies, the impedance of the gate depletion layer capacitance becomes greater than the gate isolation resistance, and the gate potential remains near ground. Therefore, in the conducting state the depletion width modulation by the gate-to-channel ac voltage is different at low and microwave frequencies, as described in detail by Jain and Gutmann [3]. While other sources of nonlinearities are present in passive MESFET switches, the change in gate ac voltage in the ON state with frequency usually dominates.

Potential users of GaAs MESFET switches in baseband or low-frequency operation should be aware that current commercial switches degrade in power handling (e.g. 1 dB signal compression, total harmonic distortion and intermodulation distortion) by about 10 dB in the range of 10–100 MHz depending upon the value of the gate bias resistor. However, recent results indicate that this decrease can be alleviated, and we expect that switches will be available in the near future with near constant power-handling capability from dc to microwave frequencies [4].

Reply[1] *by M. Schindler, M. Miller, and K. Simon*[2]

Gutmann and Jain comment on a general shortcoming of broad-band GaAs FET switches which use series FET's. Although the use of series FET's allows switches to operate at low frequencies and at dc, the series FET is also responsible for reduced power handling in this range. As Gutmann and Jain state, this limitation in low-frequency power handling is relatively well documented. Low-frequency power-handling measurements on our switches show performance degradations similar to those generally seen in this class of switch. Power handling degrades at frequencies below 50 MHz, and ultimately drops to 8 dB below power handling at microwave frequencies. Since our primary applications for these switches are for broad-band microwave systems operating above 500 MHz, this low-frequency power-handling degradation was not a concern. Nonetheless, some users may find low-frequency power handling to be critical.

Gutmann and Jain also describe the low-frequency power-limiting mechanism. To properly understand this mechanism, it is useful to refer to a detailed switch FET model, such as the one described by Gopinath and Rankin [5]. This model includes the gate-to-drain and gate-to-source capacitors in both the conducting and the nonconducting state. Although these capacitors are not generally used for modeling the conducting state, they are needed to properly understand low-frequency power handling.

Low-frequency power limiting occurs when the gate ceases to be strongly coupled to the RF path, and the gate bias resistor begins to dominate. In order to extend power handling to lower frequencies, it is desirable to maximize gate capacitances. By using the circuit design approach described in our paper, maximum gate capacitance can be accommodated for any given frequency range. This not only improves microwave performance, it also extends low-frequency power handling.

Another approach to extend power handling to lower frequencies is to increase gate bias resistor values. Our on-chip gate bias resistors have a value of 2 kΩ. When an additional 2 kΩ was inserted in the bias path (external to the MMIC), high power handling was maintained down to 20 MHz. There are, however, disadvantages to increasing bias resistance. Switching speed will be degraded, as the RC time constant is increased. There is also a limit to how high the gate bias resistance can be made. The value of gate bias resistance must be much less than any gate leakage resistance. Therefore, the use of very large value gate bias resistors can result in reduced chip yield and higher cost.

Changes in FET characteristics offer the most promising path to improving low-frequency and dc power handling. For example, a device with higher pinch-off voltage will have an advantage in low-frequency power handling. The devices we used in our $N \times M$ switches have characteristics identical to those of our standard broad-band amplifier power device. We preferred to maintain that commonality, since it allows switches and amplifiers to be readily integrated.

Gutmann and Jain further indicate that they have knowledge of a technique useful for avoiding the problem of reduced low-frequency power handling, but they fail to describe it. Since they have raised the issue, we encourage them to share any techniques they know of with the general microwave community.

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Correction to "Broad-Band Monolithic Microwave Active Inductor and Its Application to Miniaturized Wide-Band Amplifiers"

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In the above paper,[1] a small change in equation (1) is required for an accurate description of the active inductor. The correct form for (1) is

$$Z = \frac{1 + j\omega C_{gs1} R_{\mathrm{ext}}}{g_{m1} + j\omega\left[C_{gs1} - C_{gs2}\left(\frac{g_{m1}}{g_{m2}}\right) + \omega^2 C_{gs2}\left(\frac{C_{gs1}C_{gs2}}{g_{m2}^2}\right)\right]}. \quad (1)$$

When the cascode FET is composed of FET's with the same g_m and C_{gs}, the gate–source capacitances C_{gs1} and C_{gs2} cancel each other in both equations, and they result in the same equation (2). Therefore, (2) and the discussion that follows are not changed.

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